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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/694,822
Filing Date: October 29, 2003
Appellant(s): FUJII ET AL.

Liam McDowell
Reg. No. 44,231
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 01 December 2008 appealing from the Office action mailed 19 March 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claim Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Katsuki, U.S. Patent No. 5,581,767

Stokes, U.S. Patent No. 3,537,074

May, U.S. Patent No. 6,414,368

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15, 21, 23-25, 30, 32, 33 and 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuki in view of Stokes (U.S. Patent No. 3,537,074).

As per claim 15, Katsuki/Stokes discloses an array-type processor, comprising:

a multiplicity of processor elements (Fig. 1 processors 12), which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, *The examiner asserts that the processors process data and any results produced constitute event data.*

Said multiplicity of processor elements being arranged in rows and columns; *Fig. 1 shows processors 12 in rows and columns.*

A plurality of state control units that intercommunicate to realize linked operation as necessary;

An event distributing means for distributing said event data to said plurality of state control units (buses of fig. 1)

Wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data (col 12 lines 42-60 and the use of decoders suggest "code" or a preinstalled program).

Wherein each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; *The examiner asserts that each controller is connected to the one and only processor in its element area, as well as the remaining other processing elements.*

and said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units. *The examiner asserts that each controller can send data to any other controller, all of which are in other element areas. (Col. 5 lines 7-9)*

Wherein said event data are data for causing a transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit (col 7 lines 52-60 – see claim 9)

Katsuki fails to disclose a single control unit and a plurality of processor elements in each element area, in which the control units are connected to the processing elements.

Stokes discloses four control units, each dedicated to a quadrant of the processing array (col 3 line 73 to col 4 line 1).

Katsuki would have been motivated to allow for a more simplistic design that saves on cost, area, and power, but still utilizes the flexibility and efficiency described in Stokes col 2 lines 30-40).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Katsuki and expand it to four separate quadrants, each controlled by a control unit, rather than have a one-to-one correspondence to the control units and processing elements. The combination allows for four separate element areas.

Regarding claim 21, Katsuki/Stokes discloses an array-type processor in which a multiplicity of processor elements (col 5 lines 32-34), which individually execute data processing in accordance with instruction codes (col 12 lines 42-60) for which data is individually set (col 8 lines 26-29), are arranged in rows and columns (col 5 lines 47-53);

and in which a context, which is made up of said instruction codes of said multiplicity of processor elements, is switched for each operation cycle by a state control unit (col 8 lines 26-29); and in which state transitions of said multiplicity of processors elements are done while changing a configuration of said multiplicity of processor elements (col 8 lines 24-40), wherein: transitions of said operating states are done by a state control unit in accordance with a computer program that has been installed in advance and event data which are supplied by said multiplicity of processor elements (col 12 lines 42-60, also evident by the use of decoders and col 6 lines 3-10); said state control unit is composed of a plurality of units that intercommunicate to realize linked operation as necessary (col 5 lines 52-59); the multiplicity of said processor elements is divided into a number of element areas corresponding to the number of said plurality of state control units (col 5 lines 35-37); said number of element areas being less than said multiplicity of processor elements, said element areas being separate areas of said array-type processor that each have a plurality of processor elements; each of said plurality of state control units is connected to said processor elements corresponding to each of said plurality of state control units within respective element areas (col 5 liens 53-59); and said array-type processor includes an event distributing means for distributing said event data to said plurality of state control units that intercommunicate and realize linked operation (col 6 lines 7-10).

Regarding claim 23, Katsuki/Stokes discloses an array-type processor according to claim 21, wherein said event distributing means is constituted by dedicated event communication buses that connect said plurality of state control units (see claim 22).

Regarding claim 24, Katsuki/Stokes discloses an array-type processor according to claim 21, wherein: data buses for transmitting processing data of said plurality of processor elements are arranged in matrix form (col 5 lines 47-53); a plurality of switch elements, which switch-control a wiring configuration of said data buses in accordance with instruction codes that are individually set as data (col 8 lines 27-29), are arranged in matrix form together with said processor elements (fig. 2); said state control units successively switch said instruction codes of said plurality of processor elements and said plurality of switch elements (col 8 lines 26-29); and said event distributing means is constituted by said data buses that are switch-controlled by said switch elements (fig 2 references 48 and 50).

Regarding claim 25, Katsuki/Stokes discloses an array-type processor according to claim 22, wherein all of said plurality of state control units are interconnected by said event distributing means (col 5 lines 53-59).

Regarding claim 30, Katsuki/Stokes discloses an array-type processor according to claim 21, wherein an input selection means is provided for each of said state control

units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means (col 8 lines 26-29).

Regarding claim 32, Katsuki/Stokes discloses an array-type processor according to claim 21, wherein one item of said event data that has been selected by said input selection means is supplied as output to said event distributing means (fig. 2—note that the router selects both inputs and outputs to the buses).

Regarding claim 33, Katsuki/Stokes discloses an array-type processor according to claim 21, wherein output selection means is provided for each of said state control units (fig. 2), said output selection means selecting one from a plurality of items of said event data that are simultaneously received as input by said event distributing means and supplying these event data as output to said event distributing means (col 8 lines 26-29).

Regarding claim 35, Katsuki/Stokes discloses an array-type processor according to claim 21, wherein: said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area (fig. 2); each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas (fig. 2); and said event distributing means transmits said event data that are supplied as output by said processor elements

of each element area to a respective state control unit of said state control units (col 6 lines 7-9).

Claims 22, 26-29, 31 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuki/Stokes et al. (U.S. Patent No. 5,581,767) in view of May (U.S. Patent No. 6,414,368).

Regarding claim 22, Katsuki/Stokes /May discloses an array-type processor according to claim 21, wherein said event distributing means is constituted by dedicated event communication lines that connect said plurality of state control units (fig 2 reference 48 and 50).

Regarding claim 26, Katsuki/Stokes/May discloses an array-type processor according to claim 22, wherein: said plurality of state control units are arranged in rows and columns (col 5 lines 47-52); and said state control units are connected by said event distributing means to a portion of said state control units that are located in a vicinity (col 5 lines 53-59).

Regarding claim 27, Katsuki/Stokes/May discloses an array-type processor according to claim 26, wherein said state control units are connected by said event

distributing means to state control units that are located in eight directions in the vicinity (fig 1).

Examiner asserts that a control unit is connected to all other control units.

Regarding claim 28, Katsuki/Stokes/May discloses an array-type processor according to claim 26, wherein said state control units are connected by said event distributing means to said state control units that are adjacent in four row and column directions (fig 1).

Examiner asserts that a control unit is connected to all other control units.

Regarding claim 29, Katsuki/Stokes/May discloses an array-type processor according to claim 26, wherein a central control unit is provided for distributing said event data to said plurality of state control units (col 6 lines 7-9); and said central control unit is connected by said event distributing means to all of said plurality of state control units (fig. 2).

Regarding claim 31, Katsuki/Stokes/May discloses an array-type processor according to claim 26, wherein an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means (see claim 30).

Regarding claim 34, Katsuki/Stokes/May discloses an array-type processor according to claim 26, wherein: said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area (fig. 2); each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas (fig. 2); and said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units (col 6 lines 7-9).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuki in view of common art.

As per claim 9, Katsuki discloses a multiplicity of processor elements (Fig. 1 processors 12), which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, *The examiner asserts that the processors process data and any results produced constitute event data.*

Said multiplicity of processor elements being arranged in rows and columns; *Fig. 1 shows processors 12 in rows and columns.*

A plurality of state control units that intercommunicate to realize linked operation as necessary;

An event distributing means for distributing said event data to said plurality of state control units (buses of fig. 1)

a central control unit (Fig. 2 host computer 58) is provided for distributing said event data to said plurality of state control units (Col. 6 lines 7-9); and said central control unit is connected by said event distributing means to all of said plurality of state control units. *The examiner asserts that the host is connected via buses 48, 50 and 56 according to fig. 2.*

Wherein said instruction codes of said multiplicity of processor elements are successfully switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data (col 12 lines 42-60 and the use of decoders suggest "code" or a preinstalled program).

Wherein said event data are data for causing a transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit (col 7 lines 52-60)

Note that the citation shows that the transferred data includes instruction (data which causes a transition of the current state) and data (which is used for reporting to other control units the current state of a particular state control unit).

Katsuki fails to disclose that the central control unit is surrounded by said plurality of state control units.

Examiner notes that fig. 2 shows a schematic of a host computer (central control unit) that is not surrounded by the plurality of state control units. However, Examiner asserts that this drawing is only a schematic intended to show the general relationship

between processing elements and in no way teaches a determined positioning of said elements.

Examiner further asserts that the actual positioning of elements of a processing device are often determined by running a sophisticated computer program. There are many variables that this computer program has to consider, but perhaps the most paramount involves minimizing the area on which processing elements are distributed and minimizing the distance of wires between elements that commonly communicate. For this reason, it would have been obvious to allow the host computer's physical location to be "surrounded" by the state control units. This appears to be an obvious and intuitive technique for minimizing both the overall area and the wire distance for the communications. Katsuki would have been motivated to utilize this physical layout for that reason.

Allowable Subject Matter

Claim 1 is allowed.

(10) Response to Arguments

Argument with respect to Claim 9

Appellant's argument:

Figure 2 is exemplary of KATSUKI and shows a host computer 58 (offered as a control unit) connected by buses 48, 50 and 56 (offered as event distributing means) to a plurality of controllers 22 (offered as state control units). The final rejection recognizes that KATSUKI fails to disclose a central control unit surrounded by plural state control units (see page i0, last two lines). The final rejection concludes that Figure 2 of KATSUKI is a schematic drawing that is not meant

to limit the configuration of KATSUKI and that it would have been obvious to modify KATSUKI to minimize the wire distance and overall size of the device (see page 11). However, even if one of ordinary skill in the art were to consider the proposed modification, the invention of claim 9 would not result. Claim 9 specifies that a central control unit distributes said event data to said plurality of state control units. The central control unit is surrounded by said plurality of state control units and is connected by said event distributing means to all of said plurality of state control units. A configuration as recited in claim 9 centralizes the data for uniform distribution (see page 21, line 22 to page 22, line 9). KATSUKI teaches away from a configuration in which there is uniform distribution in favor of a dual bus structure with first and second bus structures that are different from each other. Column 7, lines 24-64 describe an exemplary bus structure of KATSUKI wherein the first bus structure transfers data for two immediately adjacent processor units and the second bus structure for processor units that are beyond the third nearest ones in order to provide a flexible data transfer. Thus, even if the host computer 58 as seen in Figure 2 of KATSUKI, which is offered as a central control unit, were moved to a central location as suggested in the final rejection, such modification would not result in a uniform distribution as KATSUKI requires two different bus structures. It is clear that KATSUKI is based on a bus structure with immediately adjacent elements and elements that are not immediately adjacent. KATSUKI uses a first bus structure for the immediately adjacent elements and a different second bus structure for the elements that are not immediately adjacent. See claims 1 and 14. KATSUKI does not suggest a structure other than what is explicitly shown in Figure 2. Moreover, KATSUKI could not be modified to meet the present claims. Modifying KATSUKI in the manner suggested to have a central control unit surrounded by a plurality of processors would require all the bus structures to be the same, which would change the basic principle under which KATSUKI was designed to operate, that is having two different bus structures, one for immediately adjacent elements and another for elements that are not immediately adjacent. As one of ordinary skill in the art would not be motivated to change the principle of operation of KATSUKI, the teachings of the references are not sufficient to render the claims prima facie obvious.

Examiner's response:

Before venturing too deeply into the rejection, it is important to note that Appellant has made a classic attempt to argue points that are in no way supported by the claim language. The claim language limitation in question is as follows:

...a central control unit for distributing said event data to said plurality of state control units, said central control unit is surrounded by said plurality of state control units and is connected by said event distributing means to all of said plurality of state control units....

On the basis of this claim language, Appellant states that, "[a] configuration as recited in claim 9 centralizes the data for uniform distribution." Applicant cites page 21,

line 22 to page 22, line 9 of the specification for support. Examiner fails to see any claim language that would require such a limitation, either expressly or in light of the specification. Indeed, no such language exists.

Falsely assuming that Claim 9 requires some degree of uniform distribution, Appellant proceeds to state a similarly erroneous conclusion: "Thus, even if the host computer 58 as seen in Figure 2 of KATSUKI, which is offered as a central control unit, were moved to a central location as suggested in the final rejection, such modification would not result in a uniform distribution as KATSUKI requires two different bus structures."

Indeed, on the basis of this conclusion, Appellant's flaw becomes overtly obvious. It does not matter whether the modification found in the final rejection would result in uniform distribution. The requirement merely must comply with the claim language requiring that the central control unit be "surrounded by said plurality of state control units." The prior art of record meets this limitation and Appellant does not appear to argue to the contrary. Consider the reference Chip Layout Optimization and it's related argument provided on Page 15 of the 20 June 2007 Office Action:

> *Examiner has provided the reference Chip Layout Optimization Using Critical Path Weighting. Note in the first paragraph of the introduction it states, "a good placement and routing procedure will normally try to minimize the total routing area." Moreover, Katsuki states in col 8 that "The input/output channels 56 of the host computer 58 are also connected to the column buses 48 to transfer instructions and data from the main memory (not shown) of the host computer 58 to the local memory 44 and to the instruction memory 46 of each control/memory section." Since it is obvious to minimize the total routing and the host computer must be routed to all the control/memory sections of the processor, it follows that it is obvious for the control to be physically located in the middle. This would cause the control to be surrounded by the plurality of [processing elements].*

The obviousness rejection has been properly applied in this case and the result covers the claim limitation requiring that the central control be surrounded by the plurality of state control units.

Argument with respect to Claim 15

Appellant's argument:

Claim 15 recites among other features a multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area and there is one state control unit for a plurality of processor elements. KATSUKI describes a bus structure that acts to form pairs of processor units and control/memory units in a one-to-one correspondence (see column 6, lines 10-12 and lines 32-34). STOKES discloses four control units each directly coupled to and controlling a respective processor array (plural processors). See column 3, line 73 to column 4, line i. The final rejection concludes on page 12 that: "The fact that KATSUKI mentions a one-to-one correspondence several times within the patent disclosure does not mean that it would not have been obvious to change this aspect." However, this position is contrary to one of the basic theories underlying prima facie obviousness, i.e., the suggested combination cannot change the basic principle under which the primary reference was designed to operate. In the present case, KATSUKI does not just mention a one-to-one correspondence a few times, but rather, restricts the invention to such an embodiment. At column 5, lines 32-37, KATSUKI discloses: "This invention is embodied in a bus structure ... comprising a processor ... and a control/memory section ... corresponding one-to-one to the aforementioned processor". Column 7, lines 53-56 discloses that the one-to-one correspondence accomplishes an efficient data transfer. Further, each of the claims of KATSUKI recites a one- to-one correspondence between a plurality of control/memory units and a plurality of processor units. In view of the above, it is believed to be apparent that the entire disclosure of KATSUKI is explicitly limited to and thus, based on the basic principle of operation of a one-to- one correspondence between a control unit and a processor. Modifying KATSUKI in the manner suggested to have a single control unit for a plurality of processors would change the principle of operation of KATSUKI. As one of ordinary skill in the art would not be motivated to change the principle of operation of KATSUKI, the teachings of the references are not sufficient to render the claims prima facie obvious.

Examiner's response:

A reference "teaches away" when it states that something cannot be done. *See In re Gurley*, 27 F.3d 551, 553, 31 USPQ2d 1130, 1130 (Fed. Cir. 1994). Appellant argues that the one-to-one correspondence is a basic principal of Katsuki and that its disclosure teaches away from anything other than such a relationship. To satisfy this burden, Appellant would have to show explicit language in Katsuki that a many-to-one

processor/control correspondence cannot be done. Appellant has failed to come even close to satisfying this burden.

In support of this contention, Appellant states: "As column 5, line 32-37, KATSUKI discloses: 'This invention is embodied in a bus structure – comprising a processor – and a control/memory section – corresponding one-to-one to the aforementioned processor'." Certainly, nothing in this disclosure even attempts to satisfy the burden of *In re Gurley*. At this point, all Appellant has shown is that the rejection must require an obviousness rejection, rather than an anticipatory rejection.

Appellant further states: "[c]olumn 7, lines 53-56 discloses that the one-to-one correspondence accomplishes an efficient data transfer." There are two problems with this statement. Firstly, if this is Appellant's attempt to satisfy the burden of *In re Gurley*, Appellant has fallen far short of the requirement. A mere suggestion of motivation in favor of the current implementation of a primary references in no way teaches away from the use of a secondary approach.

Secondly, Appellant has pulled this quotation completely out of context. It simply does not stand for the principal that the Brief suggests. Appellant would have us believe that the use of one-to-one correspondence results in an efficient data transfer ahead of a many-to-one correspondence. The full quotation in column 7 lines 46-62 makes it clear that this is simply not the case.

> *As described below, data transfer between processor units which are beyond the third nearest ones involve a relatively large number of relaying processor units, making the direct connection network of processors disadvantageous. Data transfers between the processor units beyond the third closest one is effected by providing 32-bit wide buses 24 on the arrays of the control/memory units 22. Thus, the transfer of instructions and data is efficiently accomplished by transferring instructions and data from a source processor to its corresponding control/memory*

unit, then transferring the values between the source and destination control/memory units via these buses and using the respective optical channel 30 to transfer the values to the destination processor unit 12 which corresponds to the destination control/memory unit 22.

Katsuki in no way states that a one-to-one correspondence is any more efficient that a many-to-once correspondence. Katsuki simply states that it is more efficient to send information to some processors in the array through a control unit rather than doing so directly. This quotation, taken in or out of context, fails to meet the burden of *In re Gurley* and nothing in this citation or elsewhere even vaguely suggests that a many-to-one correspondence would be inefficient or impossible.

Argument with respect to Claim 21

Appellant's argument:

Claim 21 includes a similar feature to that of claim 15 and recites that the multiplicity of processor elements is divided into a number of element areas corresponding to the number of state control units. The number of element areas being less than the multiplicity of processor elements. As set forth above, KATSUKI clearly requires a one-to- one correspondence between processor units and control units. The conclusion in the final rejection that KATSUKI discloses other than a one-to-one relationship between element areas/state control units and processor elements is incorrect. Moreover, claim 21 recites that a context, which is made up of said instruction codes of said multiplicity of processor elements, is switched for each operation cycle by a state control unit. Such switching the context of each operation cycle involves switching (changing) the configuration of the data paths (of the multiplicity of processor elements). In the recited array processor, the context is switched not only by the computer program, but also by the event data. In contrast, it is apparent that KATSUKI is directed to a bus architecture, which requires a bus protocol. KATSUKI is incapable of propagating the event data for each operation cycle, since KATSUKI requires operating on bus protocol. The bus protocol of KATSUKI is a combination of a first bus for adjacent processors and a second bus for long-distance ones. In view of the above, it is apparent that KATSUKI operates on a different premise than that which is recited. Accordingly, there is no factual support for the conclusion that it would have been obvious to one of ordinary skill in the art to modify KATSUKI to meet the recited configuration.

Examiner's response:

Appellant, similar to the argument of Claim 15, argues points that simply are not required by the claim language. In particular, Applicant states that "claim 21 recites that

a context, which is made up of said instruction codes of said multiplicity of processor elements, is switched for each operation cycle by a state control unit." This statement properly represents the claim language.

However, Appellant proceeds to state that "such switching the context of each operation cycle involves switching (changing) the configuration of the data paths (of the multiplicity of processor elements). In the recited array processor, the context is switched not only by the computer program, but also by the event data." This statement has, it seems, stepped beyond what the scope of the claim language can allow and ventured into the realm of obscurity.

The claim language merely requires that the instruction context information be switched for each operation cycle and that this switch occur by the state control unit. Nonetheless, Appellant states that Katsuki, in contrast, requires a bus protocol that is incapable of propagating the event data for each operation cycle. Not only does this argument, if to be found persuasive, require claim limitations that don't exist, Appellant provides no explanation or even a citation in favor of this assertion.

Appellant is, of course, incorrect in this case. No matter what definition you use for context information, it is clearly found in Katsuki's reference to Figs. 5 and 6. See col 13 line 45 to col 14 line 43. The only question is whether this occurs "for each operation cycle."

It is unclear from the claim language and Applicant's disclosure how to interpret operation cycle. In Examiner's view, an operation cycle can be properly defined as a period of time required for the control unit's router to switch connections for the data

transfers shown in Fig. 5 and 6. In this case, it would be clear that the context switches occur for each operation cycle.

However, even if operation cycle is interpreted to mean "clock cycle" (an interpretation with which Examiner does not agree) the rejection is still properly applied. Though Katsuki does not describe its data transfers in relation to clock cycles, certainly the descriptions of Figs. 5 and 6 discuss providing data to each processing unit, allowing it to execute different instructions for each cycle within a pipeline and, therefore, altering the context. If such a context was not changed every clock cycle, the processor would run into stalls and become hugely inefficient. Moreover, the system describes sending signals to communicate. Signals typically refer to electrical charges that are available on a wire only between clock cycles. In order to save signal information beyond a single clock cycle, it must be saved inside a register.

Therefore, no matter which position Appellant chooses with respect to claim interpretation, the rejection of Claim 21 is properly applied.

Examiner further notes that the Third Argument on Appeal, located on page 13 of the Brief, only asserts that May does not overcome the shortcomings of Katsuki and Stokes. This argument is moot in view of the discussion above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejection should be sustained.

Respectfully submitted,

/Brian Johnson/ Patent Examiner, Art Unit 2183

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183

/Kevin L Ellis/
Acting SPE of Art Unit 2187